

What is claimed is:

1. A differential input circuit, comprising:

a signal input terminal pair for inputting a differential input signal pair which vibrates between a first power supply potential supplied by a first power supply line and a second power supply potential supplied by a second power supply line, wherein the first power supply potential is smaller than the second power supply potential);

a first clamp circuit for generating a first control signal which depends on a higher one of one of said differential input signal pair and a first reference potential, and for generating a second control signal which depends on a lower one of said one of differential input signal pair and a second reference potential;

a second clamp circuit for generating a third control signal which depends on a higher one of the other of said differential input signal pair and said first reference potential, and for generating a fourth control signal which depends on a lower one of the other of said differential input signal pair and said second reference potential;

a first input circuit comprising a first input transistor which inputs said second control signal from a control terminal, where a first main electrode is connected to said first power supply line via a first constant current source, and a second input transistor which inputs said fourth control signal from the control terminal, where the first main electrode is

connected to said first power supply line via said first constant current source;

a second input circuit comprising a third input transistor which inputs said first control signal from the control terminal, where the first main electrode is connected to said second power supply line via a second constant current source, and a fourth input transistor which inputs said third control signal from the control terminal, where the first main electrode is connected to said second power supply line via said second constant current source;

an amplification circuit comprising a first output transistor which inputs a third power supply potential (wherein first power supply potential < third power supply potential < the second power supply potential) supplied by a third power supply line and outputs one of the differential output signals from the first main electrode; a second output transistor which inputs said third power supply potential from the control terminal and outputs the other of the differential output signals from the first main electrode; a third constant current source which supplies current received from said second power supply line to the second main electrodes of said first output transistor and said second input transistor; a fourth constant current source which supplies current received from said second power supply line to the second main electrodes of said second output transistor and said first input transistor; a fifth constant current source which emits the current received from the second main electrodes of said fourth input transistor and

said first output transistor to said first power supply line;
and a sixth constant current source which emits the current
received from the second main electrodes of said third input
transistor and said second output transistor to said first power
5 supply line; and

a bias circuit for supplying control potential, which makes
the voltage between the control electrode and the first main
electrode and the voltage between the control electrode and the
second main electrode smaller than the potential difference
10 between said first and third power supply potentials, to the
transistors constituting said first to sixth constant current
sources.

2. The differential input circuit according to Claim 1,
wherein one or a plurality of protective transistors are
15 provided between said first input transistor and said fourth
constant current source for making the voltage between the first
and second main electrodes of said first input transistor
smaller than the potential difference between said first and
third power supplies.

20 3. The differential input circuit according to Claim 2,
wherein said bias circuit supplies a control potential, which
makes the voltage between the control electrode and the first
main electrode and the voltage between the control electrode and
the second main electrode smaller than the potential difference
25 between said first and third power supplies, to a part or all of
said protective transistors.

4. The differential input circuit according to Claim 1,
wherein one or a plurality of protective transistors are
provided between said second input transistor and said third
constant current source for making the voltage between the first
5 and second main electrodes of said second input transistor
smaller than the potential difference between said first and
third power supplies.

5. The differential input circuit according to Claim 4,
wherein said bias circuit supplies a control potential, which
10 makes the voltage between the control electrode and the first
main electrode and the voltage between the control electrode and
the second main electrode smaller than the potential difference
between said first and third power supplies, to part or all of
said protective transistors.

15 6. The differential input circuit according to Claim 1,
wherein one or a plurality of protective transistors are
provided between said third input transistor and said sixth
constant current source for making the voltage between the first
and second main electrodes of said third input transistor
20 smaller than the potential difference between said first and
third power supply potentials.

7. The differential input circuit according to Claim 6,
wherein said bias circuit supplies a control potential, which
makes the voltage between the control electrode and the first
25 main electrode and the voltage between the control electrode and
the second main electrode smaller than the potential difference

between said first and third power supplies, to part or all of said protective transistors.

8. The differential input circuit according to Claim 1, wherein one or a plurality of protective transistors are provided between said fourth input transistor and said fifth constant current source for making the voltage between the first and second main electrodes of said fourth input transistor smaller than the potential difference between said first and third power supply potentials.

9. The differential input circuit according to Claim 8, wherein said bias circuit supplies a control potential, which makes the voltage between the control electrode and the first main electrode and the voltage between the control electrode and the second main electrode smaller than the potential difference between said first and third power supplies, to part or all of said protective transistors.

10. The differential input circuit according to Claim 1, wherein one or a plurality of protective transistors are provided between said third constant current source and said first output transistor for making the voltage between the first main electrode and the second main electrode of said first output transistor smaller than the potential difference between said first and third power supply potentials.

11. The differential input circuit according to Claim 1, wherein one or a plurality of protective transistors are provided between said fifth constant current source and said first output transistor for making the voltage between the first

main electrode and the second main electrode of said first output transistor smaller than the potential difference between said first and third power supply potentials.

12. The differential input circuit according to Claim 1,
5 wherein one or a plurality of protective transistors are provided between said fourth constant current source and said second output transistor for making the voltage between the first main electrode and the second main electrode of said second output transistor smaller than the potential difference
10 between said first and third power supply potentials.

13. The differential input circuit according to Claim 1, wherein one or a plurality of protective transistors are provided between said sixth constant current source and said second output transistor for making the voltage between the
15 first and the second main electrodes of said second output transistor smaller than the potential difference between said first and third power supply potentials.

14. The differential input circuit according to Claim 1, wherein said second reference potential is higher than said
20 first reference potential.

15. The differential input circuit according to Claim 1, wherein said first clamp circuit comprises:

a first transistor of a first conductive type, which inputs one of said differential input signal pair from the first main
25 electrode, and inputs said second reference potential from the control electrode, where said second main electrode is connected to the output node of said second control signal;

a second transistor of the first conductive type, which inputs said second reference potential from the first main electrodes, and inputs one of said differential input signals from said control electrode, where the second main electrode is
5 connected to the output node of said second control signal;

a third transistor of the second conductive type, which inputs one of said differential input signal pair from the second main electrode, and inputs said first reference potential from the control electrode, where the first main electrode is
10 connected to the output node of said first control signal; and

a fourth transistor of the second conductive type, which inputs said first reference potential from the second main electrode, and inputs one of said differential input signals from said control electrode, where the second main electrode is
15 connected to the output node of said first control signal.

16. The differential input circuit according to Claim 1, wherein said second clamp circuit further comprises:

a first transistor of a first conductive type, which inputs the other one of said differential input signal pair from the
20 first main electrode, and inputs said second reference potential from the control electrode, where the second main electrode is connected to the output node of said fourth control signal;

a second transistor of the first conductive type, which inputs said second reference potential from the first main
25 electrode, and inputs the other one of said differential input signal from said control electrode, where the second main

electrode is connected to the output of said fourth control signal;

a third transistor of the second conductive type, which inputs the other one of said differential input signal pair from the second main electrode, and inputs said first reference potential from the control electrode, where the first main electrode is connected to the output node of said third control signal; and

a fourth transistor of the second conductive type, which inputs said first reference potential from the second main electrode, and inputs the other one of said differential input signals from said control electrode, where the second main electrode is connected to the output node of said third control signal.

17. The differential input circuit according to Claim 1, wherein said bias circuit further comprises a plurality of stages of current mirror circuits which are connected between said first power supply line and said second power supply line, and the control terminal of transistors constituting said first to sixth constant current sources inputs the potential of the connection node between the current output terminal of each current mirror circuit and the current input terminal of the current mirror circuit in the next stage.

18. The differential input circuit according to Claim 1, wherein said first clamp circuit, said second clamp circuit, said folded cascode amplification circuit and said bias circuit are created on a complete depletion type SOI substrate.

19. The differential input circuit according to Claim 1,
wherein said first and second clamp circuits, said first and
second input circuits, said amplification circuit and said bias
circuit are constructed only with transistors which have a gate
oxide film with a film thickness having resistance against the
5 potential difference between said first power supply potential
and said third power supply potential.